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Next Generation Computing Using Quantum Dot Cellular Automata Nano Technology, New Promising Alternative to CMOS

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Abstract **- CMOS technology is one of the most popular technology in the computer chip design industry and broadly used today to form integrated circuits in numerous and varied applications and it has transformed the field of electronics. Over the time the design methodologies and processing technologies of CMOS devices have greatest activity with the Moore's law. Now CMOS technology has to face challenges to survive through the submicron ranges. The scaling in CMOS has reached higher limit, not only from technological and Physical point of view but also from economical and material aspects. This concept inspires the researches to look for new alternatives to CMOS which gives better performance and power consumption. One of the alternative technologies to digital designing in CMOS is the Quantum dot Cellular Automata (QCA). QCA is a technology it works on Electronic interaction between the cells. The QCA cell basically consists of Quantum dots separated by certain distance. The transmission of information done via the interaction between the Electrons present in these quantum dots. In this paper the limitations to CMOS in submicron range and concepts for designing in QCA have been discussed and also the building blocks are explained using QCA designer implementations with focus on cell interaction and clocking mechanism.**
Keywords: **CMOS, Moore's Law, Quantum-Dot Cellular Automata (QCA), Quantum Cell, Nanotechnology, Scaling, Clocking**

I. INTRODUCTION

The Continuous improvement in the life of human beings is due to the advancing of technologies that are developed from day to day. The most important contribution towards, the improvement of technology is the development of the field of Electronics, which largely given a new scope to it. Because of the development of the CMOS technology, there exists major revolution that forms the core of the Electronics industry. This technology has been used to the computing over the last five decades. From 1947, the first bipolar junction transistors were invented. When MOSFET's took over the improvements were occurring at a pace that was no fast. However after the evolution of CMOS, the pattern of miniaturization has achieved much exhilaration, and the scaling of CMOS completely met and satisfied this framework. The extraordinary growth in the industry over the last few decades has been due to the linear scaling which was proposed by Dennard [7]. In the basic MOS structure, the scaling of the device can be divided into two categories, the constant voltage scaling and the constant field scaling. In constant field scaling all the dimensions including the power supply voltages and the terminal voltages of the MOSFET are reduced by a same factor. From the Moore's law, he suggested in his paper [4] the number of components per integrated circuit would approximately double for every two years without increasing the cost of the Chip. This meant the type of growth would be exponential. However as suggested by the international technology & Roadmap for semiconductor ITRS, the CMOS technology has now started to face hostilities in maintaining the miniaturization criterion and holding onto the Moore's law[1-3]. The instantaneous effect of the exponential growth is the ever increasing power dissipation on a single integrated circuit. Due to the number of components keeps on increasing the power dissipation goes on increasing given a constant power handling capability of the chip. To remove this generated heat from the chip became more and more difficult as the size of the devices goes down to the sub-micron ranges. The scaling of the basic MOS structure is now reaching the quantum limitations in the possibility of further scaling has started to lose its grounds. Because of the size limitations, the dimensions of the basic device are now approaching the atomic & molecular sizes;[5,6] the possibility of further scaling of the basic device is ruled out leaving no scope for downsizing of the device.

II. LITERATURE SURVEY

A. CMOS Technology Limitations: The basic MOSFET is a device that consists of metal oxide & semiconductor, as suggested by the name itself, the structure MOS device is as shown in fig.1.

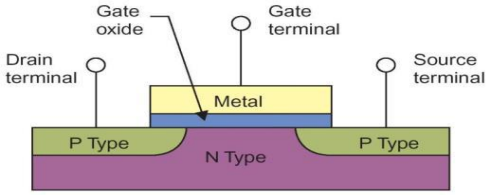


Fig. 1 Basic MOSFET Structure

The semiconductor material in the MOSFET device forms the substrate for the device action, the oxide present between metal & semiconductor is usually a dielectric which separates the substrate & the gate, the gate & the metal is the electrodes that form gate, source and drain. For the proper transition action in this device, substrate and

source drain are doped with the opposite polarity of materials resulting in the formation of opposite polarity channel with respect to the body. This is the structure of basic MOS device. The basic parameters to determine the characteristics of the device are the voltage applied to the gate terminal called as the gate-source voltage, the voltage between the drain and the source called the drain source voltage, the capacitance offered by the oxide that in the oxide capacitance, the min voltage required for the formation of the channel and the current flows between the source and the drain defined the threshold voltage.

However, the dimensions of the devices are goes down to the nanometer range, the parameters all affected by the various quantum Effects, therefore there exists by the reduction in the performance or may be the failure of the device. The limitations that the technological is facing not only include a single dimension it includes multiple viewpoints those are physical, technological, economic and the material perspectives [8]. It we consider the scaling effects, the most important one is the physical effect of this scaling. As all the dimensions of the device as scaled by the same factor both channel length and thickness of the dielectric are changed. Because of the reduction in the channel length the various channel effects come into the picture. They include the Drain induced Barrier lowering (DIBL). The high reverse bias at the drain terminal reduces the barrier faced by the carriers and allows the current to flow for voltage less than the threshold voltage of the device [9]. If the scaling reduces the oxide thickness, it approaches to the width of just a few layers of molecules. Under these size considerations, the electrons start tunneling through the oxide. Due to this the normally operated device would not allow conduction. The narrow channel of the device can also leads to merging of source and drain terminals due to the reverse bias of the drain. So it changes the basic functioning of the device. To avoid all these effects, the doping of the channel can be increased, but it also shows various effects like decrease in the mobility of the carriers so the physical dimension forms the first aspect into which the limitations of CMOS are rooted Apart from the physical aspect, the choosing of material also plays an important role in the scaling. However in the nanometer range the conventional techniques will no longer be useful. So new technologies need to be introduced to give life to CMOS. The one more important aspect in the scaling is economic perspective. Besides, smaller the size, more are the defects and the cost of overcoming them. These aspects are needed to be consider in order to implement a new technology [10,11].

III. PROPOSED METHOD

A. New Promising Alternate to CMOS Technology

To continue with the miniaturization aspects, researches have noted two important categories, firstly, the development of the CMOS related devices that extend up to 3D or vertical dimension and material technology improvement. To satisfy with the first option new materials like strained si or high k dielectrics and new structures like the multi-gate and SOI need to be studied to replace the existing designs. On the other hand transistor based paradigm shifting is the new research area. It includes a number of alternatives such as the Carbon Nanotubes, resonant tunneling devices, Single electron devices & the Quantum-dot cellular Automata Nanotechnology. These are all the new factor attracting the researchers because of the life of CMOS has to come to an end in a few decades. So an alternative, a complement for CMOS, these areas & technologies have a huge research interest in recent years [12-13].

B. Quantum-dot Cellular Automata (QCA) Nanotechnology

One of the most alternative technology developed by the researchers is the nanotechnology based Quantum-dot cellular Automate (QCA) [14]. This technology corresponds to a shift from the conventional transistor designs to designing using nano range structures like Quantum dots or metal islands. This technology works on the principles of quantum physics. It is a cellular type of a design as suggested by VonNeumann in his architectures; it was developed by C.S. Lent [14]. QCA has attracted a lot of attention due to its extremely small size & ultra-low power consumption. Present transistor based technology faces some problems like leakage current, power dissipation, oxide thickness, electron migration in feature size reduction. QCA technology solves the problem of inter connecting wires as coupling mechanism is done by columbic interaction. QCA approach provides high speed operation and avoids the problem of interconnect delay and information loss, which improves the system performance.

C. QCA Basics

1. QCA Cell: QCA cell is comprised of four quantum dots in square structure. Quantum dot is made using GaAs/ AlGaAs & Si/Sio2 materials. Electrons repel each other hence they occupy two quantum dots which are in diagonally opposite direction. Electron can tunnel from one quantum dot to other. Thus it give two stable states logic o i.e., polarization of -1 & logic 1 i.e., polarization of +1.as shown in fig.2.QCA is known as charge holder device by using a columbic repulsion method.

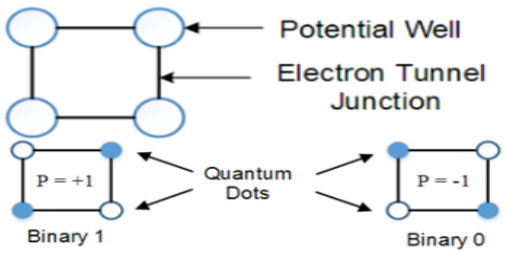


Fig. 2 QCA Cell and representation for Binary 1& 0

2. QCA Wire: QCA wire is built by using multiple number of QCA Cells in which information is transferred from one cell to adjacent cell because of Electrostatic interaction

between neighboring Cells. Depending upon the orientation of QCA cells two types of wires are available for the design of QCA circuits. Wire with 90 oriented QCA cell is shown in fig.3& second type of QCA wire with 45^0 oriented QCA cells is shown in fig.4. If wire is made using even number of 45^0 rotated cells, output will be complement of input. In other words of odd number of 45^0 rotated cells are used, output will be same as input. QCA wire with different clock Zones are used to obtain memory.

Fig. 3 QCA wire with 90^0 oriented QCA Cells

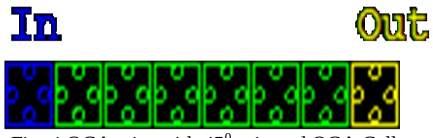


Fig. 4 QCA wire with 45^0 oriented QCA Cells

3.QCA Clock: The QCA cell itself is a computing cell, wire and storage cell. A series of QCA cells act like a wires and the signal flow is controlled by clocks. Synchronization is the important source here, so a clock plays a key role in the QCA circuit [15]. QCA clock is required in all the circuits to synchronize & control flow of information the clock actually provides the power to run the circuit [16].

4. QCA Wise Crossings: Basically QCA wire crossings are of two types, they are coplanar wire crossings and multi layer wire crossings crossing of two wires in one plane can be achieved by placing 90^0 binary wires in between 45^0 inverted wires as shown in fig.5. The two signals are able to cross each other without interference since the wires of different orientation do not have any switch effect on each other [17]. From output YA is same as input A & YB is same as input B. Hence these two wires can be treated as two different signals.

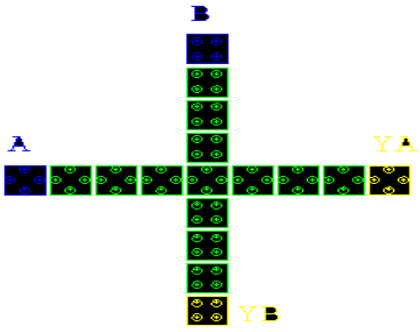


Fig. 5 Coplanar wire crossing

Multilayer wire crossing has 3 different layers that is main layer, via layer & crossover layer. The cells are placed in multiple layers so that signals can pass properly in multiple layers using vertical interconnect [18]. Multilayer wire crossings layout is shown in fig.6.

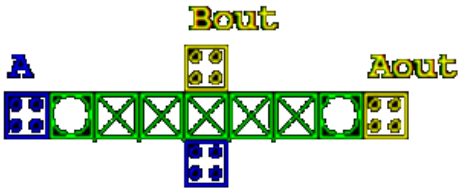


Fig. 6 Multilayer wire crossing

The basic QCA cell consists of four potential wells; these wells localize two electrons which tunnel between these due to the presence of tunnel junction. This quantum mechanical tunneling forms the basic principle of QCA designing. The second principle is the most famous law of physics that is coulomb's law. The electrons in the wells experience a columbic repulsion between them due to which the electrons in the square structure of the cell take up of only two stable configurations, these configurations are called polarizations of the cell, and the interaction between the cells forms the basic mechanism of functioning. The cells which are adjacent to each other have the ability to effect the polarization of each other. Due to the state of each cell depends on the state of the adjacent cell.

The cell provided with the input effects the cell next to it & changes its polarization to achieve a stable state with least columbic repulsions between them. In this way binary wires can be formed in QCA. The majority gate and inverter form the two more important components in QCA. The inverter is designed using the 45^0 cell at the corner in the design. Because of this shift of the cell, the least columbic forces are experienced in the cell alignment with opposite polarization and hence an inverter. The majority gate, name suggests to achieve a stable state depending on the three input values [19-20]. In this gate the central cell called as the device cell takes up the polarization of the majority of inputs to achieve a stable state. By fixing one of the input of the majority gate to zero, an OR gate can be designed. Similarly by fixing one input to one an AND gate can be realized. By combining these AND and OR gates with the inverter NAND & NOR logics can be achieved. The basic method of designing involves the conventional majority voter designing. Two more design methodologies have been suggested, one of which is based on the explicit interaction of cells and other is the tile based designs. All these designing methods are under research, some of the designs in QCA are discussed in the next section.

The correct flow of information in the QCA architecture is ensured by the clocking of circuits which is provided by the underlining CMOS or carbon nanotube wires. The function of this clocking is to provide the electric field to the QCA cells which in turn controls the raising and lowering of the barriers between the wells. If the barriers are lowered, the electrons tunnel from one well to another such that least columbic repulsion with respect to the adjacent cells. On the other hand if the barriers are raised, the electrons localize in a particular well and the tunnel junctions are closed to any movement of electrons.

In QCA, one clock cycle consists of four phases. The phases decide whether the barriers are low or high. The first is the switch phase, in which the barriers are lowered and the electrons take up a particular polarization corresponding to the neighboring cell. The next phase is the hold phase, in which the barriers are raised and no movement of electrons occurs. In this case the cell is in the position to influence the adjacent cell. Depending on the clock phase of the next cell it may either remain in the same state or change its polarization. The phase that follows the hold phase is the release and relax phase in which the barriers are again lowered and the cell again attains the null polarization. For proper working of the QCA circuits the clocking of the circuits in a proper manner is very important. The clock phases should follow each other in a proper manner otherwise the information flow can be distorted. Due to four phases, the QCA architecture is provided with four clock zones and the proper flow of information is also explained in fig.7.[21-23].

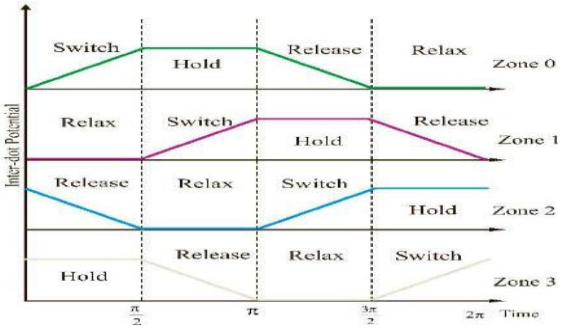
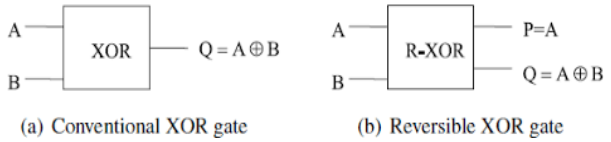


Fig. 7 Clocking Zones in QCA

D. Reversible Logic Gates

The original inspiration was that reversible gates dissipate no heat. Any reversible gate must have the same number of input and output bits. Reversible computation is achieved at a logical level by launching a one-one mapping between the input and output vectors in the logic circuit. The quantum cost of any reversible gate is calculated by counting the number of 1x1 and 2x2 quantum gates present in its design [24]. Any reversible gate can be recognized using controlled- v and controlled – v+. Fig.8 shows reversible XOR gate which is also known as Feynmen gate.



(a) Conventional XOR gate (b) Reversible XOR gate

Fig. 8 Conventional and Reversible XOR Gate

E. QCA Based Logic Generate Block (LGB)

The basic schematic of logic Generated Block LGB is shown in figure. Basic QCA logic gates like majority votes and inverter used for the implementation of LGB. The schematic and functionality of LGB is shown in fig.10, and table I respectively.

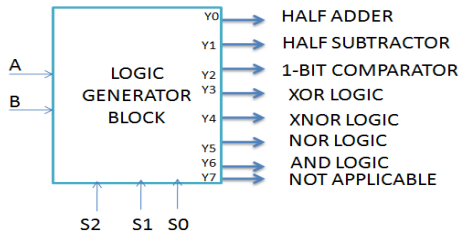


Fig. 9 Block Diagram

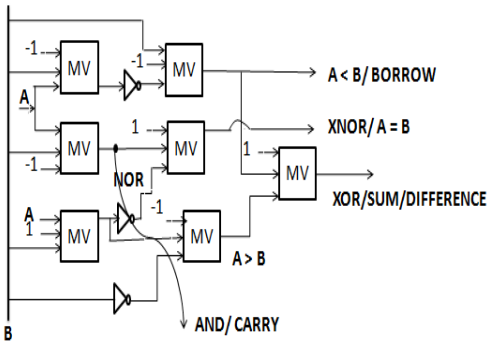


Fig. 10 Schematic of LGB using MV and NOT gate

TABLE I FUNCTIONALITY OF LGB

S. No.	Control Signals			Output of LGB
	S2	S1	S0	
1	0	0	0	1-Bit Half Adder
2	0	0	1	1-Bit Half Subtractor
3	0	1	0	1-Bit Comparator
4	0	1	1	XOR
5	1	0	0	XNOR
6	1	0	1	NOR
7	1	1	0	AND
8	1	1	1	Not Applicable

Half adder, Half Subtractor, 1- bit Comparator, XNOR logic, XOR logic, NOR logic and AND logic, is generated using single block. Functions of all the devices/components which are available at the output of LGB are basic and required for almost all the digital LGB are basic and required for almost all the digital applications like Arithmetic logic unit and in then nano-processors. Hence instead of implementing separate QCA layout for all these devices, it is better to use LGB, because the LGB is occupied less area, compared to that of total area required for the individual logic devices [24].

1-Bit Half Adder:

$$\mathrm{SUM} = \mathrm{MV}(\mathrm{MV}(\overline{\mathrm{MV}(\mathrm{A},\mathrm{B},0)},\mathrm{B},0),\mathrm{MV}(\mathrm{MV}(\mathrm{A},\mathrm{B},1),0,\overline{\mathrm{B}}),1)$$

$$\mathrm{CARRY} = \mathrm{MV}(\mathrm{A},\mathrm{B},0)$$

1-Bit Half Subtractor:

$$\mathrm{DIFFERENCE} = \mathrm{MV}(\mathrm{MV}(\overline{\mathrm{MV}(\mathrm{A},\mathrm{B},0)},\mathrm{B},0),\mathrm{MV}(\mathrm{MV}(\mathrm{A},\mathrm{B},1),0,\overline{\mathrm{B}}),1)$$

$$BORROW = MV(\overline{MV(A,B,0)},B,0)$$

1-Bit Comparator:

$$\mathrm{A} < B = MV(\overline{\mathrm{MV}(\mathrm{A},\mathrm{B},0)},\mathrm{B},0)$$

$A = B = MV(MV(A, B, 0)\overline{MV(A, B, 1)}, 1)$
$A > B = MV(MV(A, B, 1), 0, \overline{B})$
XOR Gate:
$XOR = MV(MV((\overline{MV(A, B, 0)}, MV(MV(A, B, 1), 0, \overline{B}), 1)$
NOR Gate:
$NOR = MV(A, B, 1) = \overline{A + B}$
AND Gate:
$AND = MV(A, B, 0) = A.B$

F. Reversible Logic Based Logic Generator Block

Reversible gate named XMS gate is proposed in this paper. XMS stands for XOR, Multiplexer and Sum and its block diagram is shown in fig.11. Equations of reversible XMS gate are:
P = A $\oplus$ B $\oplus$ C
Q = AB + $\overline{A}$C
R = B $\oplus$ C

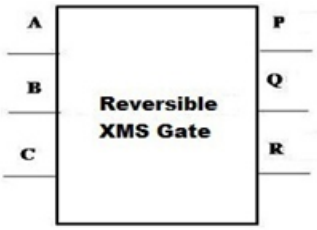


Fig. 11 Block Diagram of Reversible XMS Gate

TABLE II TRUTH TABLE OF XMS GATE

Inputs			Outputs		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	1	1	1
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	0
1	0	1	0	0	1
1	1	0	0	1	1
1	1	1	1	1	0

TABLE III FUNCTIONAL TABLE OF XMS GATE

S. No.	Control Signal			Out Put of Reversible LGB	Equation
1	A	B	C		
2	X	X	X	P = Sum of Full Adder	P=A $\oplus$ B $\oplus$ C
3	X	X	X	Q=2:1 Multiplexer	Q-A.B + $\overline{A}$C
4	X	X	X	R=2 input XOR Gate	R=B $\oplus$ C
5	X	X	1	P=2 input XNOR Gate	P=A XNOR B
6	X	X	A	Half Adder	R = A $\oplus$ B Q= AB
7	X	0	B	Half Subtractor	R = A $\oplus$ B Q= $\overline{A}$B
8	X	X	0	2 Input AND Gate	Q=AB
9	X	0	$\overline{B}$	2 Input NOR Gate	$Q = \overline{A + B}$
10	X	0	0	Pass Logic	P=A, R=B
11	X	0	$\overline{B}$	Complement	R=$\overline{B}$

IV. RESULTS

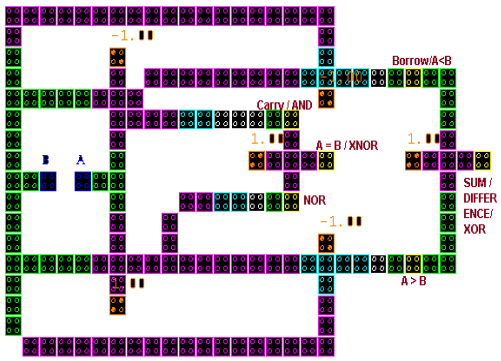


Fig.12 QCA Layout of Irreversible Logic Generator Block

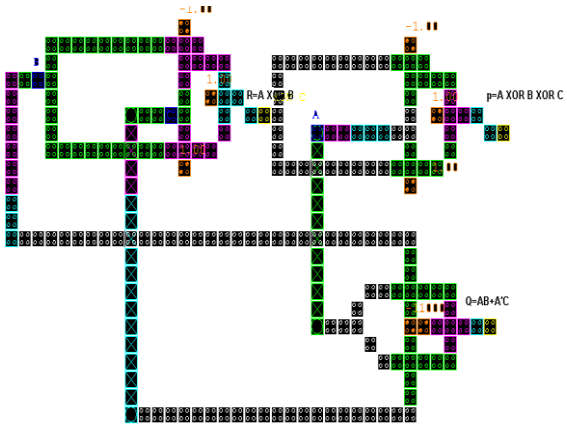


Fig. 13 QCA Layout of Reversible Logic Generator Block

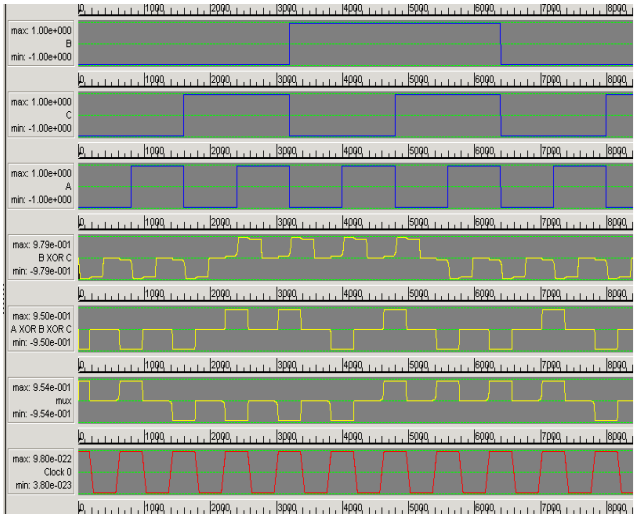


Fig. 14 Simulation Result of Reversible Logic Generator Block

V. ADVANTAGES OF QCA

QCA stands as a strong alternative or complement to CMOS due to the numerous advantages it has over the conventional CMOS technology. Some of the important advantages over CMOS involve the ultra-small size designs are possible using this technology. The basic cell in QCA is only a few nanometer scale range, thus the entire architectural area depends on the designs efficiency which are implemented.

This makes the achievement of very high density circuits in QCA which cannot be possible with the present CMOS structure. QCA technology is an edge driven one that means the input is to be applied to a single cell at the edge. The inner cells respond to the input cell and adjust their polarization. This suggests no power lines are required and the resulting architectures are ultra-low power designs. This is the most important advantage of QCA since this power dissipation is the best factor to overcome the CMOS technology.

VI. CONCLUSION

In this paper we have discussed the various limitations of the CMOS technology those are forcing the CMOS towards the end of technology. Further, we have focused on one of the promising alternative of CMOS which is the quantum dot Cellular Automata (QCA). We have discussed the basic building block in QCA, and basic working of the QCA architectures via clocking & pipelines. The various examples to understand the basic designs and the advantages of QCA over CMOS listed.

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